The LTC® 1864L/LTC1865L are 16-bit A/D converters that are offered in MSOP and SO-8 packages and operate on a single 3V supply. At 150ksps, the supply current is only 450μA. The supply current drops at lower speeds because the LTC1864L/LTC1865L automatically power down between conversions. These 16-bit switched capacitor successive approximation ADCs include sample-and-holds. The LTC1864L has a differential analog input with an external reference pin. The LTC1865L offers a software-selectable 2-channel MUX and an external reference pin on the MSOP version.

The 3-wire, serial I/O, small MSOP or SO-8 package and extremely high sample rate-to-power ratio make these ADCs ideal choices for compact, low power, high speed systems.

These ADCs can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans down to 1V full scale allow direct connection to signal sources in many applications, eliminating the need for external gain stages.

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MICROWIRE is a trademark of National Semiconductor Corporation.
LTC1864L/LTC1865L

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (VCC) ...................................................... 7V
Ground Voltage Difference
AGND, DGND LTC1865L MSOP Package ............ ±0.3V
Analog Input .................. (GND – 0.3V) to (VCC + 0.3V)
Digital Input .................. (GND – 0.3V) to 7V
Digital Output ............ (GND – 0.3V) to (VCC + 0.3V)
Power Dissipation .................. 400mW

Operating Temperature Range
LTC1864LC/LTC1865LC/ ............... 0°C to 70°C
LTC1864LAC/LTC1865LAC .......... ............... −40°C to 85°C
LTC1864LI/LTC1865LI .................. −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .............. 300°C

Storage Temperature Range ................. –65°C to 150°C

PACKAGE/ORDER INFORMATION

ORDER PART NUMBER
LTC1864LCMS8
LTC1864LIMS8
LTC1864LACMS8
LTC1864LAIMS8

ORDER PART NUMBER
LTC1865LCMS8
LTC1865LIMS8
LTC1865LACMS8
LTC1865LAAMS8

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = 25°C.
VCC = 2.7V, VREF = 2.5V, fSCK = fSCK(MAX) as defined in Recommended Operating Conditions, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1864L/LTC1865L MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>LTC1864LA/LTC1865LA MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>●</td>
<td>16</td>
<td></td>
<td>16</td>
<td></td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>No Missing Codes Resolution</td>
<td>●</td>
<td>14</td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>INL</td>
<td>(Note 3)</td>
<td>●</td>
<td>±8</td>
<td></td>
<td>±6</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Transition Noise</td>
<td></td>
<td>●</td>
<td>2</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td>LSB_RMS</td>
</tr>
<tr>
<td>Gain Error</td>
<td>●</td>
<td>●</td>
<td>±20</td>
<td></td>
<td>±20</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>
### Converter and Multiplexer Characteristics

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ C$. $V_{CC} = 2.7V$, $V_{REF} = 2.5V$, $f_{SCK} = f_{SCK\,(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1864L/LTC1865L</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
</tr>
<tr>
<td>Offset Error</td>
<td></td>
<td>±2</td>
</tr>
<tr>
<td>Input Differential Voltage Range</td>
<td>$V_{IN} = IN^+ - IN^-$</td>
<td>0</td>
</tr>
<tr>
<td>Absolute Input Range</td>
<td>$IN^+$ Input</td>
<td>−0.05</td>
</tr>
<tr>
<td></td>
<td>$IN^-$ Input</td>
<td>−0.05</td>
</tr>
<tr>
<td>$V_{REF}$ Input Range</td>
<td>LTC1864L SO-8 and MSOP, LTC1865L MSOP</td>
<td>1</td>
</tr>
<tr>
<td>Analog Input Leakage Current</td>
<td>(Note 4)</td>
<td>±1</td>
</tr>
<tr>
<td>$C_{IN}$ Input Capacitance</td>
<td>In Sample Mode</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>During Conversion</td>
<td>5</td>
</tr>
</tbody>
</table>

### Dynamic Accuracy

$T_A = 25^\circ C$. $V_{CC} = 3V$, $V_{REF} = 3V$, $f_{SAMPLE} = 150kHz$, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1864L/LTC1865L</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
<td></td>
<td>82</td>
</tr>
<tr>
<td>S/(N + D)</td>
<td>Signal-to-Noise Plus Distortion Ratio</td>
<td>1kHz Input Signal</td>
<td>82</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion Up to 5th Harmonic</td>
<td>1kHz Input Signal</td>
<td>92</td>
</tr>
<tr>
<td></td>
<td>Full Power Bandwidth</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Full Linear Bandwidth</td>
<td>$S/(N + D) \geq 75dB$</td>
<td>20</td>
</tr>
</tbody>
</table>

### Digital and DC Electrical Characteristics

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ C$. $V_{CC} = 2.7V$, $V_{REF} = 2.5V$, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>LTC1864L/LTC1865L</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage</td>
<td>$V_{CC} = 3.3V$</td>
<td>1.9</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage</td>
<td>$V_{CC} = 2.7V$</td>
<td>0.45</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current</td>
<td>$V_{IN} = V_{CC}$</td>
<td>2.5</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current</td>
<td>$V_{IN} = 0V$</td>
<td>−2.5</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{CC} = 2.7V$, $I_{O} = 10\mu A$</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 2.7V$, $I_{O} = 360\mu A$</td>
<td>2.1</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{CC} = 2.7V$, $I_{O} = 400\mu A$</td>
<td>0.3</td>
</tr>
<tr>
<td>$I_{OZ}$</td>
<td>Hi-Z Output Leakage</td>
<td>$CONV = V_{CC}$</td>
<td>±3</td>
</tr>
<tr>
<td>$I_{SOURCE}$</td>
<td>Output Source Current</td>
<td>$V_{OUT} = 0V$</td>
<td>−6.5</td>
</tr>
<tr>
<td>$I_{SINK}$</td>
<td>Output Sink Current</td>
<td>$V_{OUT} = V_{CC}$</td>
<td>6.5</td>
</tr>
<tr>
<td>$I_{REF}$</td>
<td>Reference Current (LTC1864L SO-8 and MSOP, LTC1865L MSOP)</td>
<td>$CONV = V_{CC}$</td>
<td>0.001</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{SMPL} = f_{SMPL,(MAX)}$</td>
<td>0.01</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>$CONV = V_{CC}$ After Conversion</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{SMPL} = f_{SMPL,(MAX)}$</td>
<td>0.45</td>
</tr>
<tr>
<td>$P_{D}$</td>
<td>Power Dissipation</td>
<td></td>
<td>1.22</td>
</tr>
</tbody>
</table>
## LTC1864L/LTC1865L

### Recommended Operating Conditions

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ C$.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1864L/LTC1865L</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td></td>
<td>2.7</td>
<td>3.6</td>
</tr>
<tr>
<td>$f_{SCK}$</td>
<td>Clock Frequency</td>
<td>● DC</td>
<td>8</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{CYC}$</td>
<td>Total Cycle Time</td>
<td>16 • SCK + $t_{CONV}$</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{SMPL}$</td>
<td>Analog Input Sampling Time (Note 5)</td>
<td>LTC1864L LTC1865L</td>
<td>16</td>
<td>14</td>
</tr>
<tr>
<td>$t_{SUCONV}$</td>
<td>Setup Time CONV ↓ Before First SCK ↑</td>
<td>(See Figure 1)</td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HDI}$</td>
<td>Hold Time SDI After SCK ↑</td>
<td>LTC1865L</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SDI}$</td>
<td>Setup Time SDI Stable Before SCK ↑</td>
<td>LTC1865L</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WHCLK}$</td>
<td>SCK High Time</td>
<td>$f_{SCK} = f_{SCK(MAX)}$</td>
<td>45%</td>
<td>1/$f_{SCK}$</td>
</tr>
<tr>
<td>$t_{WLCLK}$</td>
<td>SCK Low Time</td>
<td>$f_{SCK} = f_{SCK(MAX)}$</td>
<td>45%</td>
<td>1/$f_{SCK}$</td>
</tr>
<tr>
<td>$t_{WHCONV}$</td>
<td>CONV High Time Between Data Transfer Cycles</td>
<td>$t_{CONV}$</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{WLCONV}$</td>
<td>CONV Low Time During Data Transfer</td>
<td></td>
<td>16</td>
<td>SCK</td>
</tr>
<tr>
<td>$t_{HCONV}$</td>
<td>Hold Time CONV Low After Last SCK ↑</td>
<td></td>
<td>26</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Timing Characteristics

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ C$. $V_{CC} = 2.7V$, $V_{REF} = 2.5V$, $f_{SCK} = f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1864L/LTC1865L</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{CONV}$</td>
<td>Conversion Time (See Figure 1)</td>
<td>●</td>
<td>3.7</td>
<td>4.66</td>
</tr>
<tr>
<td>$f_{SMPL(MAX)}$</td>
<td>Maximum Sampling Frequency</td>
<td>●</td>
<td>150</td>
<td>kHz</td>
</tr>
<tr>
<td>$t_{DDO}$</td>
<td>Delay Time, SCK ↓ to SDO Data Valid</td>
<td>$C_{LOAD} = 20pF$</td>
<td>●</td>
<td>45</td>
</tr>
<tr>
<td>$t_{DIS}$</td>
<td>Delay Time, CONV↑ to SDO Hi-Z</td>
<td>●</td>
<td>55</td>
<td>120</td>
</tr>
<tr>
<td>$t_{DEN}$</td>
<td>Delay Time, CONV↓ to SDO Enabled</td>
<td>$C_{LOAD} = 20pF$</td>
<td>●</td>
<td>35</td>
</tr>
<tr>
<td>$t_{DIO}$</td>
<td>Time Output Data Remains Valid After SCK ↓</td>
<td>$C_{LOAD} = 20pF$</td>
<td>●</td>
<td>5</td>
</tr>
<tr>
<td>$t_{RS}$</td>
<td>SDO Rise Time</td>
<td>$C_{LOAD} = 20pF$</td>
<td></td>
<td>25</td>
</tr>
<tr>
<td>$t_{F}$</td>
<td>SDO Fall Time</td>
<td>$C_{LOAD} = 20pF$</td>
<td></td>
<td>12</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 4:** Channel leakage current is measured while the part is in sample mode.

**Note 5:** Assumes $f_{SCK} = f_{SCK(MAX)}$. In the case of the LTC1864L SCK does not have to be clocked during this time if the SDO data word is not desired. In the case of the LTC1865L a minimum of 2 clocks are required on the SCK input after CONV falls to configure the MUX during this time.
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Sampling Frequency

Reference Current vs Sampling Rate

Reference Current vs Temperature

Sleep Current vs Temperature

Reference Current vs Reference Voltage

Typical INL Curve

Typical DNL Curve

Analog Input Leakage Current vs Temperature

Supply Current vs Sampling Frequency

Reference Current vs Temperature

Sleep Current vs Temperature

Reference Current vs Reference Voltage

Typical INL Curve

Typical DNL Curve

Analog Input Leakage Current vs Temperature
PIN FUNCTIONS

LTC1864L

VREF (Pin 1): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

IN+, IN- (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

CONV (Pin 5): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this pin.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

VCC (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1865L (MSOP Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to AGND.

AGND (Pin 4): Analog Ground. AGND should be tied directly to an analog ground plane.

DGND (Pin 5): Digital Ground. DGND should be tied directly to an analog ground plane.

SDI (Pin 6): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 7): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 8): Shift Clock Input. This clock synchronizes the serial data transfer.

VCC (Pin 9): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

VREF (Pin 10): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.

LTC1865L (SO-8 Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

SDI (Pin 5): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

VCC (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. VREF is tied internally to this pin.
**LTC1864L/LTC1865L**

**FUNCTIONAL BLOCK DIAGRAM**

![Functional Block Diagram](image)

**TEST CIRCUITS**

**Load Circuit for** $t_{\text{DDO}}, t_r, t_f, t_{\text{dis}}$ and $t_{\text{en}}$

- **TEST POINT**
  - SDO

- **Voltage Waveforms for** $t_{\text{en}}$

- **Voltage Waveforms for** SDO Delay Times, $t_{\text{DDO}}$ and $t_{\text{HDDO}}$

- **Voltage Waveforms for** SDO Rise and Fall Times, $t_r, t_f$

- **Voltage Waveforms for** $t_{\text{dis}}$

**Notes:**

1. WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
2. WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.
LTC1864L OPERATION

Operating Sequence

The LTC1864L conversion cycle begins with the rising edge of CONV. After a period equal to tCONV, the conversion is finished. If CONV is left high after this time, the LTC1864L goes into sleep mode drawing only leakage current. On the falling edge of CONV, the LTC1864L goes into sample mode and SDO is enabled. SCK synchronizes the data transfer with each bit being transmitted from SDO on the falling SCK edge. The receiving system should capture the data from SDO on the rising edge of SCK. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 1.

Analog Inputs

The LTC1864L has a unipolar differential analog input. The converter will measure the voltage between the “IN+” and “IN–” inputs. A zero code will occur when IN+ minus IN– equals zero. Full scale occurs when IN+ minus IN– equals VREF minus 1LSB. See Figure 2. Both the “IN+” and “IN–” inputs are sampled at the same time, so common mode noise on the inputs is rejected by the ADC. If “IN–” is grounded and VREF is tied to VCC, a rail-to-rail input span will result on “IN+” as shown in Figure 3.

Reference Input

The voltage on the reference input of the LTC1864L defines the full-scale range of the A/D converter. The LTC1864L can operate with reference voltages from VCC to 1V.
LTC1864L/LTC1865L

APPLICATIONS INFORMATION

LTC1865L OPERATION

Operating Sequence
The LTC1865L conversion cycle begins with the rising edge of CONV. After a period equal to \( t_{\text{CONV}} \), the conversion is finished. If CONV is left high after this time, the LTC1865L goes into sleep mode drawing only leakage current. The LTC1865L’s 2-bit data word is clocked into the SDI input on the rising edge of SCK after CONV goes low. Additional inputs on the SDI pin are then ignored until the next CONV cycle. The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex). After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 4.

Analog Inputs
The two bits of the input word (SDI) assign the MUX configuration for the next requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the “+” and “−” signs in the selected row of Table 1. In single-ended mode, all input channels are measured with respect to GND. A zero code will occur when the “+” input minus the “−” input equals zero. Full scale occurs when the “+” input minus the “−” input equals \( V_{\text{REF}} \) minus 1LSB. See Figure 5. Both the “+” and “−” inputs are sampled at the same time so common mode noise is rejected. The input span in the SO-8 package is fixed at \( V_{\text{REF}} = V_{\text{CC}} \). If the “−” input in differential mode is grounded, a rail-to-rail input span will result on the “+” input.

Reference Input
The reference input of the LTC1865L SO-8 package is internally tied to \( V_{\text{CC}} \). The span of the A/D converter is therefore equal to \( V_{\text{CC}} \). The voltage on the reference input of the LTC1865L MSOP package defines the span of the A/D converter. The LTC1865L MSOP package can operate with reference voltages from 1V to \( V_{\text{CC}} \).

Table 1. Multiplexer Channel Selection

<table>
<thead>
<tr>
<th>MUX ADDRESS</th>
<th>CHANNEL #</th>
<th>GND</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINGLE-ENDED</td>
<td>0</td>
<td>+</td>
</tr>
<tr>
<td>1</td>
<td>+</td>
<td>–</td>
</tr>
<tr>
<td>DIFFERENTIAL MUX MODE</td>
<td>0</td>
<td>+</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>–</td>
</tr>
</tbody>
</table>

*After completing the data transfer, if further SCK clocks are applied with CONV low, the ADC will output zeros indefinitely.

Figure 4. LTC1865L Operating Sequence
GENERAL ANALOG CONSIDERATIONS

Grounding

The LTC1864L/LTC1865L should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a printed circuit board. The ground pins (AGND and DGND for the LTC1865L MSOP package and GND for the LTC1864L and LTC1865L SO-8 package) should be tied directly to the analog ground plane with minimum lead length.

Bypassing

For good performance, the \( V_{CC} \) and \( V_{REF} \) pins must be free of noise and ripple. Any changes in the \( V_{CC}/V_{REF} \) voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the \( V_{CC} \) and \( V_{REF} \) pins directly to the analog ground plane with a minimum of 1\( \mu \)F tantalum. Keep the bypass capacitor leads as short as possible.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1864L/LTC1865L have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source resistances are less than 200\( \Omega \) or high speed op amps are used (e.g., the LT\textsuperscript{®}1211, LT1469, LT1807, LT1810, LT1630, LT1226 or LT1215). But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

**Figure 5. LTC1865L Transfer Curve**
APPLICATIONS INFORMATION

Component Side Silk Screen for LTC1864L Evaluation Circuit

Component Side Showing Traces (Note Wider Traces on Analog Side)

Bottom Side Showing Traces (Note Almost No Analog Traces on Board Bottom)

Ground Layer with Separate Analog and Digital Grounds

Supply Layer with 5V Digital Supply and Analog Ground Repeated
**PACKAGE DESCRIPTION**

**MS8 Package**

8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660)

**RECOMMENDED SOLDER PAD LAYOUT**

**GAUGE PLANE**

**DETAIL “A”**

**NOTE:**

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

**DETAIL “A”**
PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

NOTE:
1. DIMENSIONS IN MILLIMETERS/INCHES
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)

NOTE:
1. DIMENSIONS IN MILLIMETERS/INCHES
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
TYPICAL APPLICATION

Tiny 2-Chip Data Acquisition System

LTC6910-1 (in TSOT-23 package) compactly adds 40dB of input gain range to the LTC1864L (in MSOP 8-pin package), single 3V supply.

PART NUMBER | SAMPLE RATE | POWER DISSIPATION | DESCRIPTION
--- | --- | --- | ---
LTC1860L/LTC1861L | 150ksps | 1.22mW | Pin Compatible with LTC1864L/LTC1865L
LTC1860/LTC1861 | 250ksps | 4.25mW | Pin Compatible with LTC1864/LTC1865

14-Bit Serial I/O ADCs

LTC1417 | 400ksps | 20mW | 16-Pin SSOP, Unipolar or Bipolar, Reference, 5V or ±5V
LTC1418 | 200ksps | 15mW | Serial/Parallel I/O, Internal Reference, 5V or ±5V

16-Bit Serial I/O ADCs

LTC1609 | 200ksps | 65mW | Configurable Bipolar or Unipolar Input Ranges, 5V
LTC1864/LTC1865 | 250ksps | 4.25mW | MSOP, SO-8, 1- and 2-Channel, 5V Supply

References

LT1460 | Micropower Precision Series Reference | Bandgap, 130μA Supply Current, 10ppm/°C, Available in SOT-23
LT1790 | Micropower Low Dropout Reference | 60μA Supply Current, 10ppm/°C, SOT-23

Op Amps

LT1468/LT1469 | Single/Dual 90MHz, 16-Bit Accurate Op Amps | 22V/μs Slew Rate, 75μV/125μV Offset
LT1806/LT1807 | Single/Dual 325MHz Low Noise Op Amps | 140V/μs Slew Rate, 3.5nV/√Hz Noise, –80dBc Distortion
LT1809/LT1810 | Single/Dual 180MHz Low Distortion Op Amps | 350V/μs Slew Rate, –90dBc Distortion at 5MHz