

Proposal for TCM to RCM
Data Transmission Protocol
Ver 0.9

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1 Introduction

This note describes the application of the standard SPI bus protocol to the Timing & Control Module bus which connects the TCM and RCM (Raft Control Module). The protocol described below is a slight modification of standard SPI, but well within the original intent of this bus. The bus contains the System Clock which synchronizes all Rafts and provides a data rate of ~ 50 Mbps. Actual data traffic on this bus will be exceedingly low. In addition to transmitting setup and metadata, the bus will transmit synchronous commands to all Rafts simultaneously. This feature insures strict readout synchronicity across the entire focal plane.

1.1 SPI bus signals

Signal	Function	Comment
SCLK	Serial clock	Nominal 50 MHz
SDO	Serial Data Out	Master to Slave data
SDI	Serial Data In	Slave to Master data
SYNC	Sync signal	Serial frame delimiter

Table 1

The Timing Control Module is considered the SPI bus Master, while the Raft Control Module (in BEE) is the SPI bus Slave. We will refer to this bus as the “TCM Bus”. Its signals will be LVDS and all will be “positive true”. This requires 4 signal pairs, or 8 wires.

Standard SPI bus usage calls for the Master to send SCLK signals only when necessary. In our case, the TCM sends SCLK continuously. This signal serves as the timebase for the focal plane readout.

In standard SPI usage, the SS (Slave Select) line is used in typical fashion as a Chip Select. In our usage, it has been renamed SYNC and will be used to delimit (initiate) a data transfer. It therefore serves to synchronize operation of all Rafts.

1.2 Bus Transfer TYPEs

Transactions on the TCM Bus will be defined by TYPE as follows.

TYPE	Function	Code (hex)
WRT (16 bit)	Master to Slave data transfer	0
WRT (special)	Ditto but non-16-bit length	1
READ (16 bit)	Slave to Master Data Transfer	2
READ (special)	Ditto but non-16-bit length	3
XQT	Execution statement	4
-	Reserved	5 – F

Table 2

As the TYPE field is a 4-bit field, there is plenty of space for additional types to be added as need.

1.3 RCM (Raft Control Module) address space.

The RCM will contain a frame buffer capable of storing image data for one CCD. This corresponds to 16 Megapixels or 16 MWords¹. There is no need to make this address space available on a word by word basis. It will be addressable as 16k “pages” of 1k words per page. In the case of a segmented sensor with 0.5k x 2k pixels per sensor, each page corresponds to two rows of the segment. Pages will be read as block transfers. Memory test data may be downloaded also as pages.

Total addressable memory space will be 64kWords. There will be no Byte addressing. The address field will generally be 16 bits wide, each pointing to a unique WORD address. WRT(special) and READ(special) TYPES are reserved for word lengths other than 16-bits, should we decide to implement them. This might be the case if, for example, the ADCs used to digitize the video signal are 18-bit devices and it is determined that we want to keep all 18 bits.

The upper 16k locations are reserved for Frame Buffer page addresses. See memory map below.

Address range	Function
E000 - FFFF	Frame buffer page addresses
C000 - DFFF	Command space
A000 - BFFF	Setup registers and metadata
0000 – 9FFF	State machine code & registers

Table 3

1.4 Data format

Each data transfer will consist of a Header followed, in the case of READs or WRITEs, by one or more data words.

Rule: For purposes of insuring robust data transmission at both sending and receiving ends, both Header and DATA words will be bracketed at the leading edge by a “1” and at the trailing edge by a “0”. As the TCM bus is a very low data rate bus, the overhead for this rule will be negligible.

4-bits	16-bits	12-bits
TYPE	ADDRESS	COUNT

COUNT is a 12-bit word indicating the number of words to be transferred in a BLOCK Transfer. Single word transfers correspond to the special case where the COUNT field is equal to “1”.

ADDRESS is a 16-bit field corresponding to a 64k bit address space. TYPE is a 4-bit field corresponding to the TYPES defined in Table 2.

¹ A “WORD” in this context is defined as 2 Bytes, or 16 bits.

1.5 TCM Bus Timing

1.5.1 WRITE Operations

The following timing diagram shows a 16 bit WRT with frame delimiters (leading “1”s and trailing “0”s) bracketing the Header and Data words.

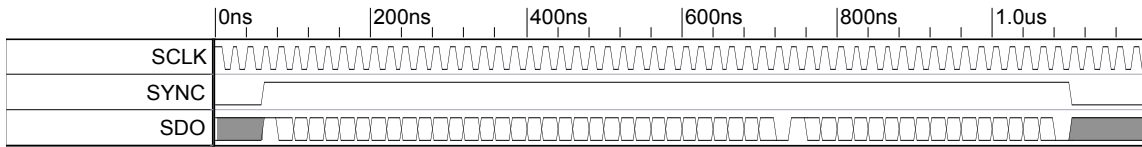


Figure 1 – WRITE Operation

BLOCK WRITE operations are identical to the above, except that the SS line is kept high throughout the operation. Each additional data word is bracketed by leading 1 and trailing 0.

Timing detail for a WRITE operation is shown below. The SPI Master registers all signals using its SCLK line (50 MHz). The driven signals, SYNC and SPO are thus delayed by one propagation delay, T_p , from the SCLK edges. The SCLK and SDO are received at the SLAVE where FPGA buffers guarantee that the CLK buffer is faster than the DATA buffers by a few nanoseconds and is generally programmable in the devices. This guarantees that the data setup time at the SLAVE’s registers is very close to a clock period, or just under 20 ns. Having programmed the clock and data delays at the device outputs and inputs, one can forget this detail and simply assume the data will be latched in on the **subsequent** clock edge.

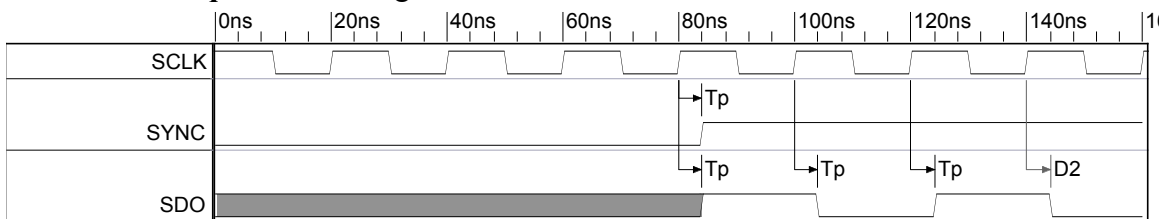


Figure 2 - Timing detail

RULE : After terminating an operation, the Master must insure at least 4 SCLK cycles before initiating another one.

1.5.2 READ Operation

READ operations are complicated by the cable and prop delays between TCM and RCM. In principle, the round trip propagation delay can be determined by the Master during a “delay learning mode”. In typical FPGA devices, this can be done to a fraction of a nanosecond. Having learned the delay, the Master assumes it is present in all Read commands and adjusts the phase of its Read Clock accordingly. **It is the responsibility**

of the Master to perform this learning operation to insure correct data phase while reading data from the Slaves.

In addition to the round trip delay, upon receipt of a READ command, it may take the SLAVE several clock cycles to retrieve the data. The additional leading “1” takes care of this issue. **In a Read operation, the Slave must keep the SDI line False (0) until the first data word is ready, at which time it presents the leading edge “1” as a frame delimiter.**

1.6 Execution (XQT) commands.

These are commands which are executed synchronously by the RCM upon receiving the header alone. No additional data transfers are involved and the command to be executed is indicated by the address field in the header. A simple example would be the synchronous reset of an on-board timing counter in the RCM. Sending this command to all RCMs simultaneously would insure that all rafts have identical time information. Needless to say, the most important function of such a command would be to issue the START READOUT command to the Raft Controller’s “Readout State Machine”. In this way, all rafts maintain their CCD readout cycles in strict synchronicity.

